REMARKS

Claims 5-11, 50-52, and 55-62 are all the claims presently being examined in the application. Applicant has respectfully canceled claims 53 and 54 without prejudice or disclaimer.

Claims 5-11 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,252,271.

Claims 5, 8-11, 50, 52, 55-57, and 59-61 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamazaki, et al. (U.S. Patent No. 5,633,519). Claims 5, 8-11, 50, 52, 55-57, and 59-61 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yang (U.S. Patent No. 5,258,634). Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki, et al. in view of Wake (U.S. Patent No. 5,338,953). Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang in view of Wake. Claims 7 and 58 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki, et al. Claims 7 and 58 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yang.

These rejections are respectfully traversed in view of the following discussion.

It is noted that the amendments are made only to more completely define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example by claim 5, and somewhat similarly by independent claim 62, is directed to a memory structure.

The memory includes a gate conductor including a first side and a second side where the first side includes a slope and the second side includes a substantially vertical sidewall, and at least one floating gate includes polysilicon spacer material and is formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides. Importantly, the slope includes an angle of taper between about 45^0 and about 65^0. (See Page 5, line 18-Page 6, line 22; Page 7, line 6-Page 8, line 4; and Figures 1-7, 8A, 8B, 10A and 10B).

Conventional memory cell structures include a floating gate defined by a trim mask or polysilicon spacers formed on both sidewalls using an "added-on floating gate." However, the conventional structures tend to increase lithographic alignment problems, "require good control of the overlay for the spacer removal mask," prevent down-scaling of "large cell sizes," add extra process steps and materials, and thus increases manufacturing costs. (See Page 1, line 17-Page 2, line 30).

An aspect of the memory structure includes a sloped first sidewall where the slope includes an angle of taper between about 45^0 and about 65^0. This allow spacers to be formed on only the non-sloped edge of the wordlines, and thereby eliminates the trim mask as appropriate sections of the wordline along the floating gate edge are tapered and provide tapered regions

between the floating gates. Thus, the floating gates can be isolated with no additional masks. (Page 6, lines 2-22).

As a result of this invention, the resultant structure supports self-alignment and "minimizes alignment concern for high density device integration" as well as provides for the floating gate to be "fabricated to an extremely small size and is self-isolated from adjacent FG [floating gate] devices by the gate conductor." The structure can be formed using less steps and material, and thus reduces manufacturing costs. (See Page 3, line 1-Page 4, line 8).

II. THE OBVIOUSNESS-TYPE DOUBLE PATENTING REJECTION

A. The Obvious-Type Double Patenting Rejection Based on U.S. Patent No. 6,252,271

First, Applicant traverses the obviousness-type double patenting rejection based on claims 1-6 of U.S. Patent No. 6,252,271. In particular, Applicant's present invention is a Divisional Application of U.S. Patent Application 09/097,515 (Parent Application), filed on June 15, 1998, which issued as Patent No. 6,252,271. Applicant elected to file the Divisional Application for claims 5-11 as the Examiner made a Restriction Requirement previously indicated that claims 5-11 of the Parent Application represented a different invention than the invention defined by claims 1-4 of the same Parent Application, which issued as U.S. Patent No. 6,252,271. Since claims 1-4 and 5-11 of the Parent Application were considered to be two different inventions, the two sets of claims can not now represent the same invention, and thus Applicant traverses the obvious-type double patenting rejection.

Secondly, the Examiner is prohibited from reading limitations from the specification into

the applied patent claims. Accordingly claims 1-6 of Patent No. 6,252,271 B1 do not make Applicant's invention obvious. Claims 1-6 of '271 indicate, in part, that "a second sidewall having, a second slope angle greater than said first slope angle" and "at least one floating gate is partially surrounded on a plurality of sides by said second sidewall."

In contrast, the plain language of claim 5 of Applicant's invention indicates, in part, that "the first side includes a slope and the second side includes a substantially vertical sidewall and at least one floating gate which includes comprising polysilicon spacer material and formed on the second side of the gate conductor such that the gate conductor surrounds at least one floating gate on a plurality of sides where the slope includes an angle of taper between about 45^0 and about 65^0." Nowhere does the '271 Patent indicate "a substantially vertical sidewall," "the gate conductor surrounds at least one floating gate," or "the slope includes an angle of taper between about 45^0 and about 65^0." Therefore, as indicated above, the '271 Patent does not make Applicant's invention obvious.

III. PRIOR ART REJECTIONS

A. The Yamazaki, et al. Reference

Regarding claims 5, 8-11, 50, 52, 55-57 and 59-61, Yamazaki, et al. ("Yamazaki") fails to teach or suggest the features of independent claim 5, including the slope includes an angle of taper between about 45^0 and about 65^0. (See Page 5, line 18-Page 6, line 22; Page 7, line 6-Page 8, line 4; and Figures 1-7, 8A, 8B, 10A and 10B).

Indeed, the Examiner admits that Yamazaki does "not disclose regions are tapered." (See

Office Action, Page 8, Section 4).

Instead, Figures 1(A)-1(B) and 3(E) as well as Figures 7(A), 7(B), 8(A) and 8(B) of Yamazaki teach a non volatile floating gate semiconductor including a floating gate and a control gate formed on a sidewall. In particular, this structure actually forms a double sidewall where the floating gate (what the Examiner attempts to analogize to a gate conductor with a first side having a slope) is formed without the use of a sloped sidewall, and thus the floating gate is not self-aligned. Based on this vertical structure, the source and drain regions are formed on different levels. Accordingly, this non-volatile floating gate is a symmetric structure with a floating gate and a control gate formed "with the gate extending beyond the lower edge of the floating gate electrode," compared to just a floating gate formed on a side of a gate conductor where the other side of the gate conductor includes a sloped surface as recited in Applicant's invention. (See Office Action, Page 3, Section 2; Yamazaki at Abstract; Column 5, lines 15-22; Column 12, lines 24-40; and Figures 1(A)-1(B), 3(E), 7(A), 7(B), 8(A) and 8(B)).

Since, as indicated above, the Examiner admits that Yamazaki does not disclose "regions are tapered," Yamazaki certainly does not disclose or teach including a slope with an angle of taper, let alone, the slope includes an angle of taper between about 45^0 and about 65^0 as claimed in Applicant's invention.

Accordingly, the gate conductor includes a first side, which is sloped, i.e., tapered, and has an angle of taper between about 45^0 and about 65^0, whereas Yamazaki teaches a floating gate and a control gate formed on the sidewall to produce a double sidewall where the floating gate is formed without use of a sloped sidewall, let alone, the slope includes an angle of taper between

about 45^0 and about 65^0.

B. The Yang Reference

Regarding claims 5, 8-11, 50, 52, 55-57 and 59-61, Yang ("Yang") also fails to teach or suggest the features of independent claim 5, including the slope includes an angle of taper between about 45^0 and about 65^0. (See Above).

Indeed, the Examiner admits that Yang does "not disclose regions are tapered." (See Office Action, Page 9, Section 5).

Instead, Figures 5C-8 of Yang teach an electrically erasable read only memory cell array having an elongated control gate in a trench. In particular, at least one floating gate 17 is formed in the trench 12 with a second insulating layer 22 formed over the floating gate electrode and "a second polycrystalline layer 24 is deposited in overlying relation to gates in trench, ..., [T]wo different configurations of layer, which will serve as a control gate." Accordingly, "[t]his leaves a gate electrode that extends substantially the length of the trench in overlying relation to floating gates. This structure actually forms a double sidewall where the floating gate is formed without use of a sloped sidewall, and the floating gate may not be self-aligned. Further, based on this structure, the source and drain regions are formed on different levels. (See Yang at Abstract; Column 2, line 60 - Column 3, line 45; and Figures 5(A)- 8). Accordingly, this memory cell array is a symmetric structure with a floating gate and a control gate formed in a trench compared with just a floating gate formed on a side of a gate conductor where the other side of the gate conductor includes a sloped surface as disclosed by Applicant's invention.

Since, as indicated above, the Examiner admits that Yang does not disclose "regions are tapered," Yang does not disclose or teach including a slope with an angle of taper, let alone, the slope includes an angle of taper between about 45^0 and about 65^0 as recited in Applicant's invention.

C. The § 103(a) Rejection of Claim 6

To make up for the deficiencies of Yamazaki and Yang, the Examiner relies on Wake ("Wake"). Wake fails to do so.

First, Wake, which pertains to "an electrically erasable and programmable semiconductor memory device having an improved writing efficiency, does not have the same aim as Yamazaki, as discussed above, and the urged combination would not have been made, absent hindsight. (See Wake at Abstract; Column 1, lines 10-20; and Column 4, lines 24-30). Applicant asserts that Yamazaki, as indicated above, in part, is a non-volatile floating gate semiconductor device focused on reducing the number of mask processes and the required accuracy of the mask processes whereas Wake's electrically erasable and programmable semiconductor memory device includes an improved writing efficiency. Thus, the two references teach against being combined.

Similarly, Wake, as indicated above, does not have the same aim as Yang, as discussed above, and the urged combination would not have been made, absent hindsight. (See Yang at Abstract; Column 1, lines 10-45). Applicant asserts that Yang, as indicated above, in part, is an EPROM cell capable of providing a means to increase the density and number of cell array devices and memory cells on a semiconductor chip. (Yang at Abstract; and Column 1, lines 10-

45) whereas Wake's electrically erasable and programmable semiconductor memory device includes an improved writing efficiency. Thus, the two references teach against being combined.

Secondly, Yamazaki and Yang, do "not disclose regions are tapered." (See Office Action, Page 8, Section 4; and Page 9, Section 5).

Third, Wake does not disclose, teach or suggest, including the slope includes an angle of taper between about 45^0 and about 65^0, as recited in independent claim 5.

Further, Wake does not disclose, teach or suggest, including the gate conductor which is formed on a silicon substrate, and adjacent ones of at least one floating gate are isolated from each other and the second sidewall includes tapered regions provided between the adjacent one of at least one floating gate as recited in claim 6 of the invention.

Instead, Figures 3 and 18 of Wake teaches an electrically erasable and programmable semiconductor memory device with a trench memory transistor where a floating gate electrode is formed on a first gate oxide film and a second gate oxide film in a trench. Further, "[a] control gate electrode is formed over [the] floating gate electrode with layer insulating film there between." In particular, "[a] pair of memory transistors M is formed in each trench. Memory transistor M includes floating gate electrode 5, control gate electrode 7, n+ -drain diffusion region 2 and n+ -source diffusion region 3." (See Wake at Abstract; Column 7, lines 20-35; and Column 8, lines 37-47). Accordingly, Wake teaches a floating gate and a control gate formed in a trench to produce a double sidewall structure whereas Applicant teaches that the floating gate, itself, is formed on the gate conductor where the gate conductor, i.e., control gate, surrounds the floating gate as a result of the notching process.

Contrary to the assertion in the Office Action, the gate conductor 7, according to Figure 3,

appears to include a non-vertical side portion, but is more structurally and functionally equivalent to a non-tapered side not a tapered side as suggested in the Office Action. Indeed, the assertion in the Office Action that Wake discloses "an angle is between about 45 degrees to 60 degrees" is murky, at best. The Office Action fails to cite the particular portion of the Wake reference, which may be relied upon to teach this feature, consistent with 37 C.F.R. Section 1.104(c)(2) requiring that "the particular part relied on must be designated as nearly as practicable." (See MPEP 707.5). Accordingly, the Applicant respectfully asserts that the Examiner has mischaracterized Wake because Wake does not teach or disclose that the gate conductor 7 includes a slope including an angle of taper between about 45^0 and about 65^0. Thus, Applicant traverses this general rejection of previous dependent claim 54 now incorporated into independent claim 5. (See Office Action, Page 8, Section 4).

Further, please note, the Office Action incorrectly suggest that Wake teaches a range between 45 degrees to 60 degrees, which it does not as indicated above, as teaching Applicant's invention. When, in fact, Applicant's claimed invention teaches a range between 45 degrees to 65 degrees.

Indeed, Wake's electrically erasable and programmable semiconductor memory device is primarily focused on providing an improved writing efficiency. (See Column 4, lines 24-40). Since this programmable semiconductor memory device includes a floating gate and a control gate in a trench to form a double sidewall type structure but the sidewall, as discussed above, but does not include the slope includes an angle of taper between about 45^0 and about 65^0, Wake is deficient and thus does not teach the specific limitation of independent claim 5.

For the reasons stated above, the claimed invention, and the invention as cited in

independent claim 5, and related dependent claim 6, should be fully patentable over the cited references.

D. The § 103(a) Rejection of Claim 7 and 58 over Yamazaki, et al.

Regarding claims 7 and 58 , Yamazaki, as discussed above, does not disclose, teach or suggest, including the slope includes an angle of taper between about 45^0 and about 65^0, as recited in independent claim 5.

Further, Yamazaki does not disclose, teach or suggest, including the gate conductor surrounds at least one floating gate on only two sides as recited in claim 7 of the invention. Yamazaki also does not disclose, teach or suggest, including the gate conductor is covered by a dielectric comprising a thickness in a range of about 100 nm to 1,000 nm.

Since the Examiner admits that Yamazaki "does not disclose the gate conductor surrounds [the] at least one floating gate on only two sides,"and "does not disclose regions are tapered," certainly, this non-volatile floating gate semiconductor device, which includes a floating gate and a control gate formed on a side surface to produce a double sidewall type structure, does not include the slope includes an angle of taper between about 45^0 and about 65^0. (See Office Action, Page 7, Section 8; and Page 8, Section 4). Accordingly, Yamazaki is deficient and thus does not teach the specific limitations of dependent claims 7 and 58.

For the reasons stated above, the claimed invention, and the invention as cited in independent claim 5, and related dependent claims 7 and 58, should be fully patentable over the cited reference.

E. The § 103(a) Rejection of Claims 7 and 58 over Yang

Regarding claims 7 and 58, Yang, as discussed above, does not disclose, teach or suggest, including the slope includes an angle of taper between about 45^0 and about 65^0, as recited in independent claim 5.

Further, Yang does not disclose, teach or suggest, including the gate conductor surrounds at least one floating gate on only two sides as recited in claim 7 of the invention. Yang also does not disclose, teach or suggest, including the gate conductor is covered by a dielectric comprising a thickness in a range of about 100 nm to 1,000 nm.

Since the Examiner admits that Yang "does not disclose the gate conductor surrounds [the] at least one floating gate on only two sides," and "does not disclose regions are tapered," certainly, this non-volatile floating gate semiconductor device, which includes a floating gate and a control gate formed on a side surface to produce a double sidewall type structure, does not include the slope includes an angle of taper between about 45^0 and about 65^0. (See Office Action, Page 7, Section 8; and Page 8, Section 4). Accordingly, Yang is deficient and thus does not teach the specific limitations of dependent claims 7 and 58.

For the reasons stated above, the claimed invention, and the invention as cited in independent claim 5, and related dependent claims 7 and 58, should be fully patentable over the cited reference.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 5-11, 50-52, and 55-62, all the claims presently being examined in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

Date: 2/19/04

Fredric J. Zimmerman, Esq.
Reg. No. 48,747

McGinn & Gibb, PLLC
8321 Old Courthouse Rd., Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254